Patent claims

1. A method for generating a trigger signal (A) according to the current differential protection principle in the case of a fault on a section (E) of an electrical power supply system, in which

- differential current values (id) are monitored with regard to exceeding a predetermined lower limit value of the differential current (id) (differential current limit value (igu)) and also with regard to exceeding stabilization current values (is) weighted with a characteristic curve factor (K), and
- the trigger signal (A) is generated if positive results of the two instances of monitoring are present simultaneously,

characterized in that

- the differential current values (id) and the stabilization current values (is) are calculated with instantaneous values of the currents (i1, i2) detected at the section (E) of the electrical power supply system, as instantaneous values,
- a first measurement quantity (isd), which is proportional to the differential quotient of the stabilization current (is) with respect to time, is formed and checked in an evaluation operation to determine whether this first measurement quantity (isd) exceeds a predetermined limit value of the differential quotient of the differential current with respect to time (differential current quotient limit value (igd1),
- a second measurement quantity (idd), which is proportional to the differential quotient of the differential current (id) with respect to time, is formed and checked in a further evaluation operation to determine whether the second measurement quantity

(idd) exceeds the differential current quotient limit value (igd1), and

- the trigger signal (A) is generated if the two evaluation operations produce positive results at the same time as the two instances of monitoring.

2. The method as claimed in claim 1,
characterized in that

- a check is made to determine whether the first measurement quantity (isd) is greater than the second measurement quantity (idd), and, if appropriate, the trigger signal (A) is generated.

3. The method as claimed in claim 1 or 2,
characterized in that
a check is made to determine whether the second measurement quantity (idd) exceeds the first measurement quantity (isd) weighted with the characteristic curve factor (K), and, if appropriate, the trigger signal (A) is generated.

4. The method as claimed in one of the preceding claims,
characterized in that

- the smallest value (ismin) of the stabilization current (is) is determined in each case in a time range in which the first measurement quantity (isd) becomes less than zero,
- its largest value (ismax) is determined in each case in a time range in which the first measurement quantity (isd) becomes greater than zero, and
- a check is made to determine whether the stabilization current (is) is greater than KMIN times the smallest value (ismin), where $1 < KMIN < \sqrt{2}$, and 0.5 times the value of the largest value (ismax), and,

- if appropriate, the trigger signal (A) is generated.

5. The method as claimed in one of the preceding claims,
characterized in that
- the trigger signal (A) is generated if the evaluation operations and the instances of monitoring have yielded positive results Ns times in succession, where Ns is freely selectable.

6. The method as claimed in claim 5,
characterized in that
- in the absence of Ns results, the trigger signal (A) is generated when at least the instances of monitoring have produced positive results Nz times, where Ns << Nz.

7. The method as claimed in one of the preceding claims,
characterized in that,
in the absence of a trigger signal (A), an internal inhibit signal (B) is generated if
- the first measurement quantity (isd) is greater than the limit value of this quantity (igd2),
- furthermore the second measurement quantity (idd) is less than the instantaneous value - weighted with the k factor - of the first measurement quantity (k*isd) and, at the same time, the instantaneous value of the stabilization current (is) is greater than
- a limit value (ish),
- a first reweighted limit value (idg/k),
- a second reweighted limit value (1.5*idg), and
- a comparison value calculated as mean value from previous values (isrms comparison value).

8. The method as claimed in claim 7,

characterized in that

- after the generation of an inhibit signal, a trigger signal is generated only when the instances of monitoring and/or the instances of evaluation have produced a positive result at least Nz times.

9. A current differential protection arrangement for a section (E) of an electrical power supply system having

- a measured value preprocessing device (MV), in which respective differential current values (id) and stabilization current values (is) respectively assigned thereto are formed continuously from currents (i1, i2) detected at the ends of the section (E), having
- an evaluation device (AW) connected downstream of the measured value preprocessing device (MV),
  - in which evaluation device the differential current (id) is checked to determine whether it exceeds a predetermined differential current limit value (idg), and having
- a logic circuit (L1), which, on the input side, is connected to the evaluation device (AW) and has an output for outputting a trigger signal (A),

characterized in that

the measured value preprocessing device (MV) is designed in such a way that it generates differential current instantaneous values and stabilization current instantaneous values (is),

- a first limit value stage (Gs) is arranged downstream of a first differentiator (Ds), to which stabilization current instantaneous values (is) are applied, which limit value stage is also connected to a differential current quotient limit value transmitter (G1) on the input side,
- a second limit value stage (Gd) is arranged downstream of a second differentiator (Dd), to which

differential current instantaneous values are applied, which limit value stage is also connected to the differential current quotient transmitter (G19) on the input side, and

- the logic circuit (L1) is arranged downstream of the limit value stages and generates the trigger signal (A) when output signals of the limit value stages are present.

10. The current differential protection arrangement as claimed in claim 9,
characterized in that

- a first comparator (K1) is connected to the two differentiators (Dd, Ds) and, on the output side, is connected to the logic circuit (L1).

11. The current differential protection arrangement as claimed in claim 7 or 8,
characterized in that

- a second comparator (K2) is indirectly arranged downstream of the first differentiator (Ds) via a translation stage (U1) and of the second differentiator (Dd) and is connected to the logic circuit (L1) on the output side.

12. The current differential protection arrangement as claimed in one of claims 9 to 11,
characterized in that

- provision is made of a determination device (U) for the smallest value (ismin) of the stabilization current (is),
- a weighting device (BE) is connected to the determination device (U), and
- a comparison stage (VS) is arranged downstream of the weighting device (BE), to which comparison stage, on the input side, the stabilization current

instantaneous values (is) are also applied and which comparison stage is connected to the logic circuit (L1) on the output side.

13. The current differential protection arrangement as claimed in one of claims 9 to 12,
characterized in that

- a comparison stage (V1) is arranged downstream of a transmitter (G1g) for the differential current quotient limit value (idg) and a second transmitter (G2) for the stabilization quotient limit value (igf), which comparison stage is connected to the logic circuit (L1) on the output side,
- a further comparison stage (V2) is connected, on the input side, on the one hand to the input of the first differentiator (Ds) and on the other hand, via a further translation stage (U2), to a transmitter (G1g) for the limit value (idg) of the differential current (id) and is connected to the logic circuit (L1) on the output side,
- a third comparison stage (V3) is connected, on the input side, on the one hand to the output of the first differentiator (Ds) and on the other hand to the output of the further transmitter (G2) and is connected to the logic circuit (L1) on the output side,
- a fourth comparison stage (V4) is connected, on the input side, on the one hand to the input of the second differentiator (Dd) and on the other hand, via a third translation stage (U3), to the input of the first differentiator (Ds) and is connected to the logic circuit (L1) on the output side, and
- a fifth comparison stage (V5) is connected, on the input side, on the one hand to the output of the second differentiator (Dd) and on the other hand, via a fourth translation stage (U3), to the output of the

first differentiator (Ds) and is connected to the logic circuit (L1) on the output side.